1. An electrically modifiable memory, comprising:
a first matrix of memory cells, each of which is capable of storing at least two information bits, the first matrix being divided into sectors;
an address circuit, coupled to the first matrix, for addressing the memory cells in the first matrix;
a programming circuit, coupled to the first matrix, for programming the memory cells in the first matrix;
a read circuit, coupled to the first matrix, for reading from the memory cells in the first matrix;
a write circuit, coupled to the first matrix, for writing to the memory cells in the first matrix;
a control circuit, coupled to the first matrix, the address circuit, the programming circuit, the read circuit, and the write circuit;
a refresh circuit, coupled to the control circuit and receiving periodic clock pulses, the refresh circuit activating an operation to refresh the memory cells of the first matrix in response to the periodic clock pulses; and
a second matrix of static memory cells, the second matrix of static memory cells containing memory values that are stored in a first sector of the first matrix while the first sector is being refreshed, so that the memory values of the first sector may be accessed from the second matrix while the first sector is being refreshed.

2. The electrically modifiable memory of claim 1, wherein the operation to refresh the memory cells is preformed sector by sector.

3. The electrically modifiable memory of claim 1, further comprising:
a second address circuit, coupled to the second matrix, for addressing the static memory cells in the second matrix;
wherein the operation to refresh the memory cells is performed in a duplication step for the duplication, in the second matrix, of information elements contained in a sector of the first matrix, and a refresh step for refreshing the memory cells of the first matrix containing the set of information elements.

4. The electrically modifiable memory of claim 3, wherein the second matrix includes a number of static memory cells that is equal to a number of non-volatile memory cells in a sector of the first matrix.

5. The electrically modifiable memory of claim 1, wherein the refresh operation is performed substantially every hour.

6. The electrically modifiable memory of claim 1, wherein each of the memory cells in the first matrix includes a non-volatile memory cell.

7. The electrically modifiable memory of claim 1, further comprising a clock circuit, coupled to the refresh circuit, that provides the periodic clock pulses to the refresh circuit.

8. The electrically modifiable memory of claim 1, further comprising an address comparator, coupled to the an address circuit, the address comparator receiving an address from an external circuit for a memory cell to be accessed and an address defining a sector to be refreshed, and providing as an output a signal indicative of whether the memory cell to be accessed is within the sector to be refreshed.

9. The electrically modifiable memory of claim 1, wherein the read circuit includes an output indicative of whether a memory cell has an output current at a magnitude indicative that correction of data within the memory cell is valid.

10. A method for operating a memory, comprising the steps of:
receiving a clock input;
in response to the clock input, determining that a refresh operation for a first group of a plurality of groups of memory cells within the memory will be performed; and
performing the refresh operation for the first group of the plurality of groups of memory cells;
wherein, in response to the memory losing power, a value from the clock input is stored in nonvolatile memory.

11. The method of claim 10, wherein each of the first group of memory cells includes a memory cell that stores multiple bits of data.

12. The method of claim 10, further comprising the steps of:
generating the clock input; and
in response to power being applied to the memory, re-initializing the clock input to the value that was stored in the non-volatile memory.

13. The method of claim 10, further comprising the steps of:
determining that the refresh operation for the first group of memory cells is complete; and
response to the refresh operation for the first group of memory cells being complete, performing a refresh operation for a second group of the plurality of groups of memory cells within the memory.

14. The method of claim 10, further comprising the step of transferring data from the first group to a storage area that is different from the first group of memory cells, so that the storage area may be accessed during the refresh operation of the first group of memory cells.

15. The method of claim 14, further comprising the step of accessing the storage area during the refresh operation to obtain the data that was previously stored in the first group of memory cells.

16. The method of claim 15, further comprising the steps of:
determining whether a memory access request is directed to a cell within the first group of memory cells while the first group of memory cells is being refreshed;
when the memory access request is directed to a cell within the first group of memory cells, accessing the storage area; and
when the memory access request is not directed to a cell within the first group of memory cells, accessing a second group of memory cells.

17. The method of claim 14, wherein the first group of memory cells is in a first memory matrix, and the storage area is in a second memory matrix that is different from the first memory matrix.

18. The method of claim 10, wherein the step of performing the refresh operation for the first group includes the steps of:

determining a read current from one of the first group of memory cells;

in response to a magnitude of the read current, determining that a refresh will be performed; and

refreshing by re-writing a value into the one of the first group of memory cells.

19. A method for operating a memory, comprising the steps of:

detecting that a refresh operation is activated for a first group of memory cells within the memory;

transferring data from the first group of memory cells to a second group of memory cells so that the second group of memory cells may be accessed during the refresh operation of the first group of memory cells; and

transferring data from the second group of memory cells back to the first group of memory cells subsequent to the refresh operation of the first group of memory cells.

20. The method of claim 19, wherein each of the first group of memory cells is capable of storing a plurality bits of data, the method further comprising the step of refreshing each of the first group of memory cells.

21. The method of claim 20, wherein the step of refreshing includes the steps of:

determining a read current from one of the first group of memory cells;

in response to a magnitude of the read current, determining that a refresh will be performed; and

performing the refresh by re-writing a value into the one of the first group of memory cells.

22. The method of claim 19, further comprising the step of accessing the second group of memory cells during the refresh operation to obtain the data that was previously stored in the first group of memory cells.

23. The method of claim 19, further comprising the steps of:

determining whether a memory access request is directed to a cell within the first group of memory cells while the first group of memory cells is being refreshed;

when the memory access request is directed to a cell within the first group of memory cells, accessing the second group of memory cells to respond to the memory access request; and

when the memory access request is not directed to a cell within the first group of memory cells, accessing the second group of memory cells to respond to the memory access request.

24. The method of claim 19, wherein the first group is in a first memory matrix, and the second group of memory cells is in a second memory matrix that is different from the first memory matrix.

25. An apparatus for operating a memory, comprising:

means, operative in response to a clock input, for determining that a refresh operation for a first group of a plurality of groups of memory cells within the memory will be performed;

means for performing the refresh operation for the first group of the plurality of groups of memory cells;

means, operative in response to the memory losing power, for storing a value from the clock input in non-volatile memory.

26. The apparatus of claim 25, wherein each of the first group of memory cells includes a memory cell that stores multiple bits of data.

27. The apparatus of claim 25, further comprising:

means for generating the clock input; and

means, operative in response to power being applied to the memory, for re-initializing the clock input to the value that was stored in the non-volatile memory.

28. The apparatus of claim 26, further comprising:

means for determining that the refresh operation for the first group of memory cells is complete; and

means, operative in response to the refresh operation for the first group of memory cells being complete, for performing a refresh operation for a second group of the plurality of groups of memory cells within the memory.

29. The apparatus of claim 25, further comprising means for transferring data from the first group to a storage area that is different from the first group of memory cells, so that the storage area may be accessed during the refresh operation of the first group of memory cells.

30. The apparatus of claim 29, further comprising means for accessing the storage area during the refresh operation to obtain the data that was previously stored in the first group of memory cells.

31. The apparatus of claim 30, further comprising:

means for determining whether a memory access request is directed to a cell within the first group of memory cells while the first group of memory cells is being refreshed;

means for accessing the storage area when the memory access request is directed to a cell within the first group of memory cells, and

means for accessing a second group of memory cells, when the memory access request is not directed to a cell within the first group of memory cells.

32. The apparatus of claim 29, wherein the first group of memory cells is in a first memory matrix, and the storage area is in a second memory matrix that is different from the first memory matrix.

33. The apparatus of claim 25, wherein the means for performing the refresh operation for the first group includes:

means for determining a read current from one of the first group of memory cells;

means, operative in response to a magnitude of the read current, for determining that a refresh will be performed; and

means for refreshing by re-writing a value into the one of the first group of memory cells.

34. An apparatus for operating a memory, comprising:

means for detecting that a refresh operation is activated for a first group of memory cells within the memory;

means for transferring data from the first group of memory cells to a second group of memory cells so that the second group of memory cells may be accessed during the refresh operation of the first group of memory cells; and

means for transferring data from the second group of memory cells back to the first group of memory cells subsequent to the refresh operation of the first group of memory cells.

35. The apparatus of claim 34, wherein each of the first group of memory cells is capable of storing a plurality bits of data, the apparatus further comprising means for refreshing each of the first group of memory cells.

36. The apparatus of claim 35, wherein the means for refreshing includes:

means for determining a read current from one of the first group of memory cells;

means, operative in response to a magnitude of the read current, for determining that a refresh will be performed; and

means for performing the refresh by re-writing a value into the one of the first group of memory cells.

37. The apparatus of claim 34, further comprising means for accessing the second group of memory cells during the refresh operation to obtain the data that was previously stored in the first group of memory cells.

38. The apparatus of claim 34, further comprising:

means for determining whether a memory access request is directed to a cell within the first group of memory cells while the first group of memory cells is being refreshed;

means for accessing the second group of memory cells to respond to the memory access request when the memory access request is directed to a cell within the first group of memory cells, and

means for accessing the second group of memory cells to respond to the memory access request when the memory access request is not directed to a cell within the first group of memory cells.

39. The apparatus of claim 34, wherein the first group is in a first memory matrix, and the second group of memory cells is in a second memory matrix that is different from the first memory matrix.

40. A memory apparatus comprising:

a plurality of memory cells arranged in a plurality of groups of memory cells;

a refresh control circuit having an input that receives a clock signal and an output that provides a signal indicative that a refresh operation will be performed on a first group of the plurality of groups of memory cells within the memory apparatus;

a refresh circuit, having an input that receives the indicator signal and an output that controls the refresh operation for the first group of the plurality of groups of memory cells; and

a storage area that is different from the first group of memory cells, the storage area storing data that was previously stored in the first group of memory cells, so that the storage area may be accessed during the refresh operation of the first group of memory cells.

41. The memory apparatus of claim 40, wherein each of the first group of memory cells includes a memory cell that stores multiple bits of data.

42. The memory apparatus of claim 40, further comprising:

a clock generator having an output that provides the clock signal to the input of the refresh control circuit, the clock generator; and

a storage circuit, coupled to the clock generator, that stores a clock signal value from the clock generator in response to the memory losing power.

43. The memory apparatus of claim 40, wherein the refresh control circuit is constructed and arranged to perform a refresh operation for a second group of the plurality of groups of memory cells within the memory apparatus in response to the refresh operation for the first group of memory cells being complete.

44. The memory apparatus of claim 40, wherein the first group of memory cells is in a first memory matrix, and the storage area is in a second memory matrix that is different from the first memory matrix.

45. The memory apparatus of claim 40, further comprising a comparator circuit having a first input that receives an address indicative of a memory access request, a second input that receives an address indicative of the first group of cells, the comparator providing as an output a signal indicative of whether the memory access request is directed to a cell within the first group of memory cells while the first group of memory cells is being refreshed.

46. The memory apparatus of claim 40, wherein:

the refresh circuit has an input that receives a read current from one of the first group of memory cells; and

the refresh circuit determines whether a refresh will be performed based upon a magnitude of the read current.

47. A memory apparatus, comprising:

a first group of memory cells;

an indicator circuit that provides a signal indicative that a refresh operation is activated for the first group of memory cells;

a second group of memory cells, distinct from the first group of memory cells, the second group of memory cells storing data from the first group of memory cells so that the second group of memory cells may be accessed during the refresh operation of the first group of memory cells.

48. The memory apparatus of claim 47, wherein each of the first group of memory cells is capable of storing a plurality bits of data, the apparatus further comprising a refresh circuit having an output that refreshes each of the first group of memory cells.

49. The memory apparatus of claim 48, wherein:

the refresh circuit has an input that receives a read current from one of the first group of memory cells; and

the refresh circuit determines whether a refresh will be performed based upon a magnitude of the read current.

50. The memory apparatus of claim 47, further comprising a read circuit having an output that accesses the second group of memory cells during the refresh operation to obtain the data that was previously stored in the first group of memory cells.

51. The memory apparatus of claim 47, further comprising a comparator circuit having a first input that receives an address indicative of a memory access request, a second input that receives an address indicative of the first group of cells, the comparator providing as an output a signal indicative of whether the memory access request is directed to a cell within the first group of memory cells while the first group of memory cells is being refreshed.

52. The memory apparatus of claim 47, wherein the first group is in a first memory matrix, and the second group of memory cells is in a second memory matrix that is different from the first memory matrix.

53. A method for operating a memory, comprising steps of:

detecting that a refresh operation is activated for a first group of memory cells within the memory; and

transferring data from the first group of memory cells to a storage area that is different than the first group of memory cells so that the data from the first group of memory cells may be accessed during the refresh operation of the first group of memory cells.

54. An apparatus for operating a memory, comprising:

means for detecting that a refresh operation is activated for a first group of memory cells within the memory; and

means for transferring data from the first group of memory cells to a storage area that is different than the first group of memory cells so that the data from the first group of memory cells may be accessed during the refresh operation of the first group of memory cells.